What is claimed is:

1. A semiconductor device, comprising:

bonding pads that are formed on a semiconductor substrate;

an upper copper layer that is formed on the lower surface of said bonding pads with a barrier metal interposed; and

a lower copper layer that is formed closer to said semiconductor substrate than said upper copper layer;

wherein a copper area of said lower copper layer under said bonding pads is equal to or lower than that of said upper copper layer.

2. A semiconductor device according to claim 1, wherein said lower copper layer is electrically insulated from said upper copper layer.

3. A semiconductor device according to claim 1, wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, wherein said

upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, further comprising:

interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and

via-plugs composed of copper that are embedded in said interlevel dielectric films;

wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, wherein said lower copper layer is constituted by a plurality of copper layers.

12. A semiconductor device according to claim 11, wherein the copper area ratio of each of the copper layers of said lower copper layer are equal.

13. A semiconductor device according to claim 11, wherein dielectric films that are composed of a first material are interposed between each of the copper layers of said lower copper layer.

14. A semiconductor device according to claim 13, wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

15. A semiconductor device according to claim 14, wherein said second material is softer than said first material.

16. A semiconductor device according to claim 14, wherein a dielectric film that is composed of said second material contains any one of: a SiOC film, a silicon carbide (SiC) film, a SiOF film, a porous silicon dioxide (SiO_2) film, a porous SiOC film, and a ladder oxide film having a ladder-type hydrogenated siloxane.

17. A semiconductor device according to claim 13, wherein dielectric films composed of a third material having a lower relative dielectric constant than said first material are interposed between each of the copper

layers of said lower copper layer.

18. A semiconductor device according to claim 17, wherein said third material is softer than said first material.

19. A semiconductor device according to claim 17, wherein a dielectric film composed of said third material contains any one of; a SiOC film, a silicon carbide (SiC) film, a SiOF film, a porous silicon dioxide (SiO_2) film, a porous SiOC film, and a ladder oxide film having a ladder-type hydrogenated siloxane.

20. A semiconductor device, comprising:
bonding pads that are provided on a semiconductor substrate;
an upper copper layer that is formed on the lower surface of said bonding pads with a barrier metal interposed; and
a lower copper layer that is formed closer to said semiconductor substrate than said upper copper layer;
wherein said upper copper layer is electrically insulated from said lower copper layer, and the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

21. A semiconductor device according to claim 20, wherein the copper area ratio of said upper copper layer is at least 70%.

22. A semiconductor device according to claim 20, wherein the

planar dimensions of said bonding pads and said upper copper layer are substantially the same.

23. A semiconductor device according to claim 20, wherein said upper copper layer is constituted by a plurality of copper layers.

24. A semiconductor device according to claim 23, wherein the copper area ratios of each of the copper layers of said upper copper layer are the same.

25. A semiconductor device according to claim 23, further comprising:
interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and
via-plugs composed of copper that are embedded in said interlevel dielectric films;
wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

26. A semiconductor device according to claim 25, wherein a copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and via-plugs that are connected to this copper layer pattern are embedded in a dielectric film that is composed of a first material.

27. A semiconductor device according to claim 20, wherein the copper area ratio of said lower copper layer is at least 15% and not greater

than 95%.

28. A semiconductor device according to claim 20, wherein said lower copper layer is constituted by a plurality of copper layers.

29. A semiconductor device according to claim 28, wherein the copper area ratios of each of the copper layers of said lower copper layer are the same.

30. A semiconductor device according to claim 28, wherein dielectric films that are composed of a first material are interposed between each of the copper layers of said lower copper layer.

31. A semiconductor device according to claim 30, wherein each of the copper layers of said lower copper layer is constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

32. A semiconductor device according to claim 31, wherein said second material is softer than said first material.

33. A semiconductor device according to claim 31, wherein dielectric films composed of said second material contain any one of; a SiOC film, a silicon carbide (SiC) film, a SiOF film, a porous silicon dioxide (SiO_2) film, a porous SiOC film, and a ladder oxide film having a ladder-type hydrogenated siloxane.

34. A semiconductor device according to claim 30, wherein dielectric films composed of a third material having a lower relative dielectric constant than said first material are interposed between each of the copper layers of said lower copper layer.

35. A semiconductor device according to claim 34, wherein said third material is softer than said first material.

36. A semiconductor device according to claim 34, wherein said dielectric films composed of said third material contain any one of: a SiOC film, a silicon carbide (SiC) film, a SiOF film, a porous silicon dioxide (SiO_2) film, a porous SiOC film, and a ladder oxide film having a ladder-type hydrogenated siloxane.

37. A semiconductor device according to claim 20, wherein said barrier metal contains titanium nitride (TiN) or tantalum nitride (TaN).

38. A semiconductor device according to claim 20, further comprising:

internal circuits that are provided on said semiconductor substrate; and

auxiliary copper interconnects that is electrically connected to said internal circuits;

wherein said auxiliary copper interconnects are electrically connected to a portion of said bonding pads by way of via-holes.

39. A method of fabricating the semiconductor device described in claim 1, wherein said upper copper layer and said lower copper layer are formed by a damascene method.

40. A method of fabricating the semiconductor device described in claim 9, wherein a copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and via-plugs that are connected to this copper layer pattern are formed by a dual damascene method.

41. A method of fabricating the semiconductor device described in claim 26, wherein a copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and via-plugs that are connected to this copper layer pattern are formed by a dual damascene method.